Design and Implementation of MIMO-STBC Systems on FPGA Hardware

Bui Huu Phu

DCSELAB, Hochiminh City University of Technology, Vietnam

Email: bhphu@dcselab.edu.vn

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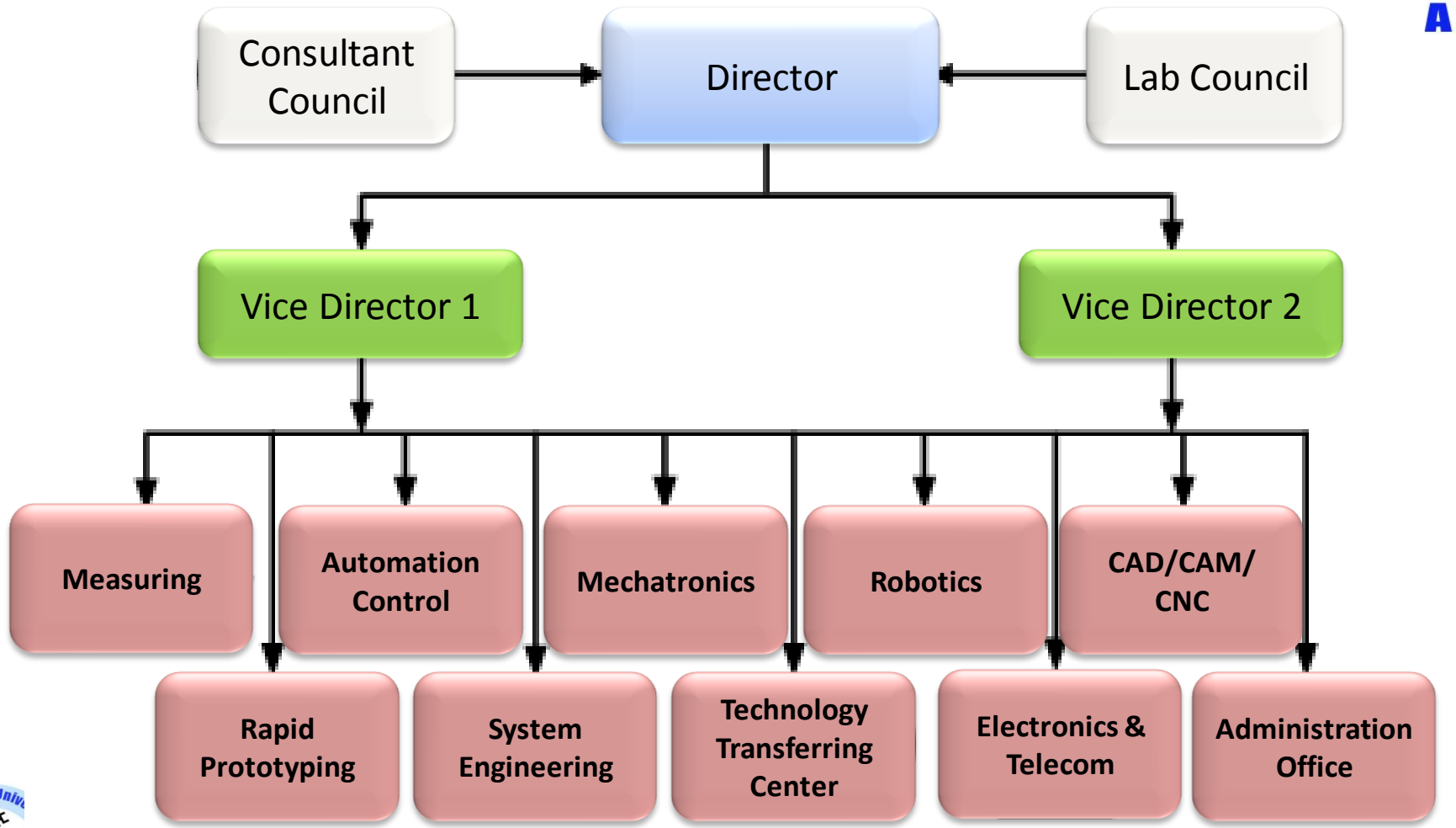
Organization chart



AB

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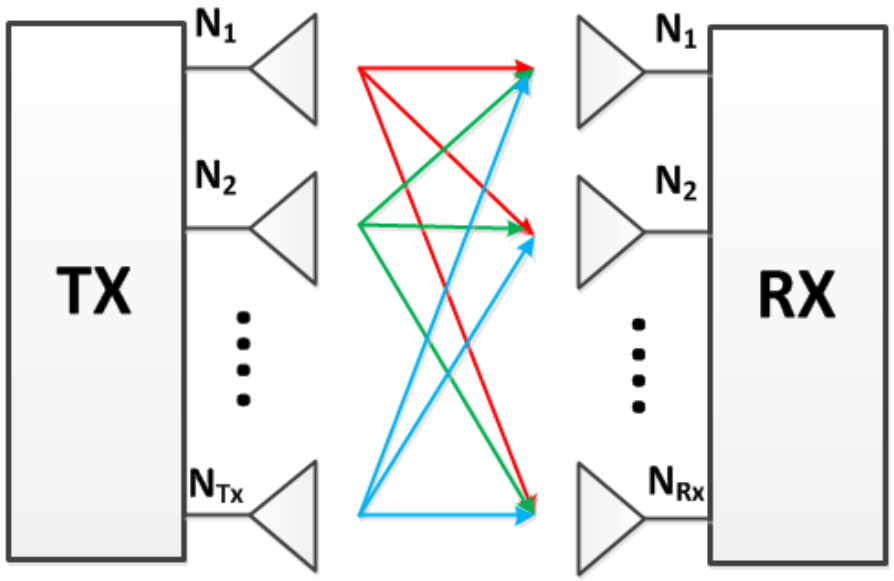
Outline of Presentation

1. Introduction of MIMO SDM systems
2. Design of system on FPGA hardware
   - Transmistter side
   - MIMO flat fading channel
   - Receiver side
3. Experimental results
   - BER performance of designed systems
   - Hardware Consumption
4. Conclusion

Overview of MIMO SDM Systems



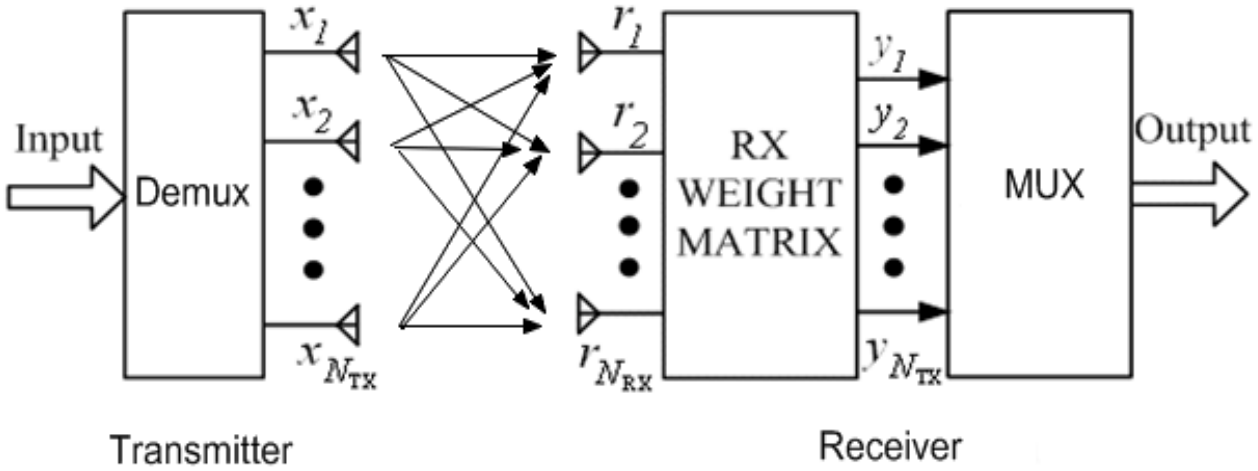
MIMO Systems

MIMO equalization methods are generally categorized into:

- A high-quality transmission: a transmission of a single data stream
- A high data rate transmission: a transmission of multiple data sub-streams

In the paper, we focus on the second type, space division multiplexing (SDM).

Overview of MIMO SDM Systems



MIMO SDM Systems

$$\boldsymbol{r}(t) = \boldsymbol{H}\boldsymbol{x}(t) + \boldsymbol{n}(t),$$

$$r_i(t) = \sum_{j=1}^{N_{TX}} h_{ij} x_j(t) + n_i(t).$$

$$\boldsymbol{H} = \begin{pmatrix} h_{11} & h_{12} & \cdots & h_{1N_{TX}} \\ h_{21} & h_{22} & \cdots & h_{2N_{TX}} \\ \vdots & \vdots & h_{ij} & \vdots \\ h_{N_{RX}1} & h_{N_{RX}2} & \cdots & h_{N_{RX}N_{TX}} \end{pmatrix},$$

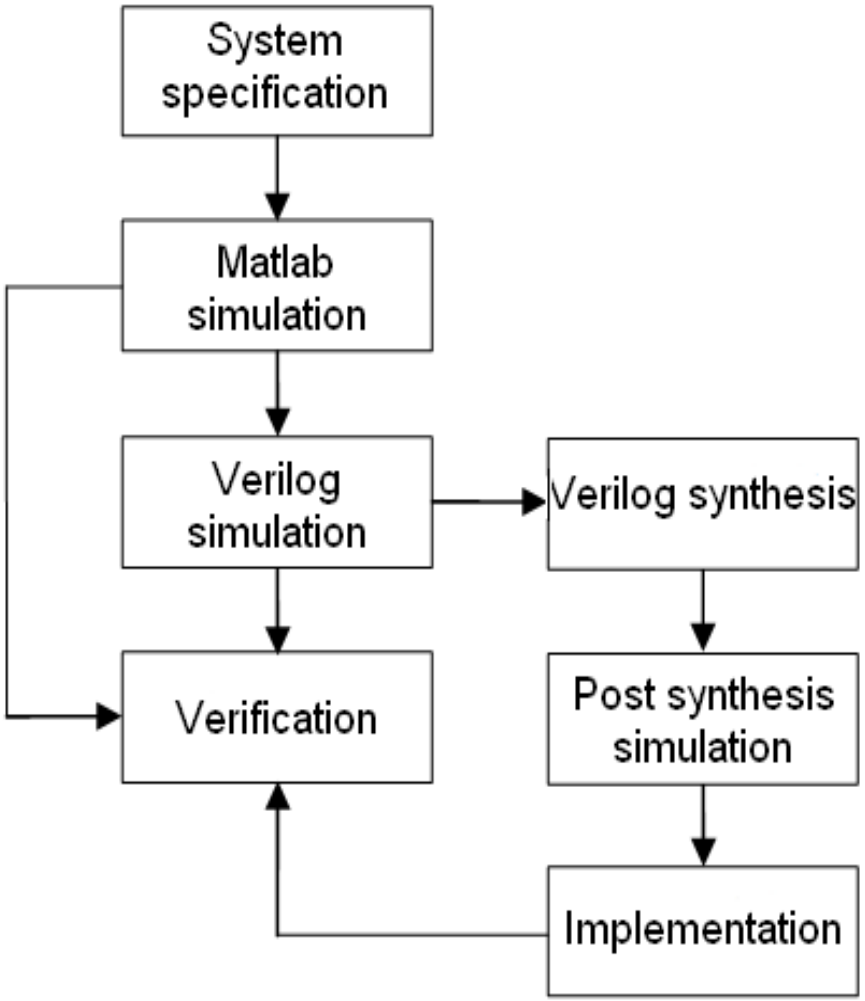
Problems and Motivations

- Until now, many technical papers have been evaluated the MIMO SDM systems based on theory analyses and/or computer-based simulations.
- Just few ones fully considered the systems on FPGA hardware design, an important step before going to make ICs.
- In the paper, we present our design and implementation of MIMO SDM systems on FPGA hardware, then show the consumptions of resource elements.

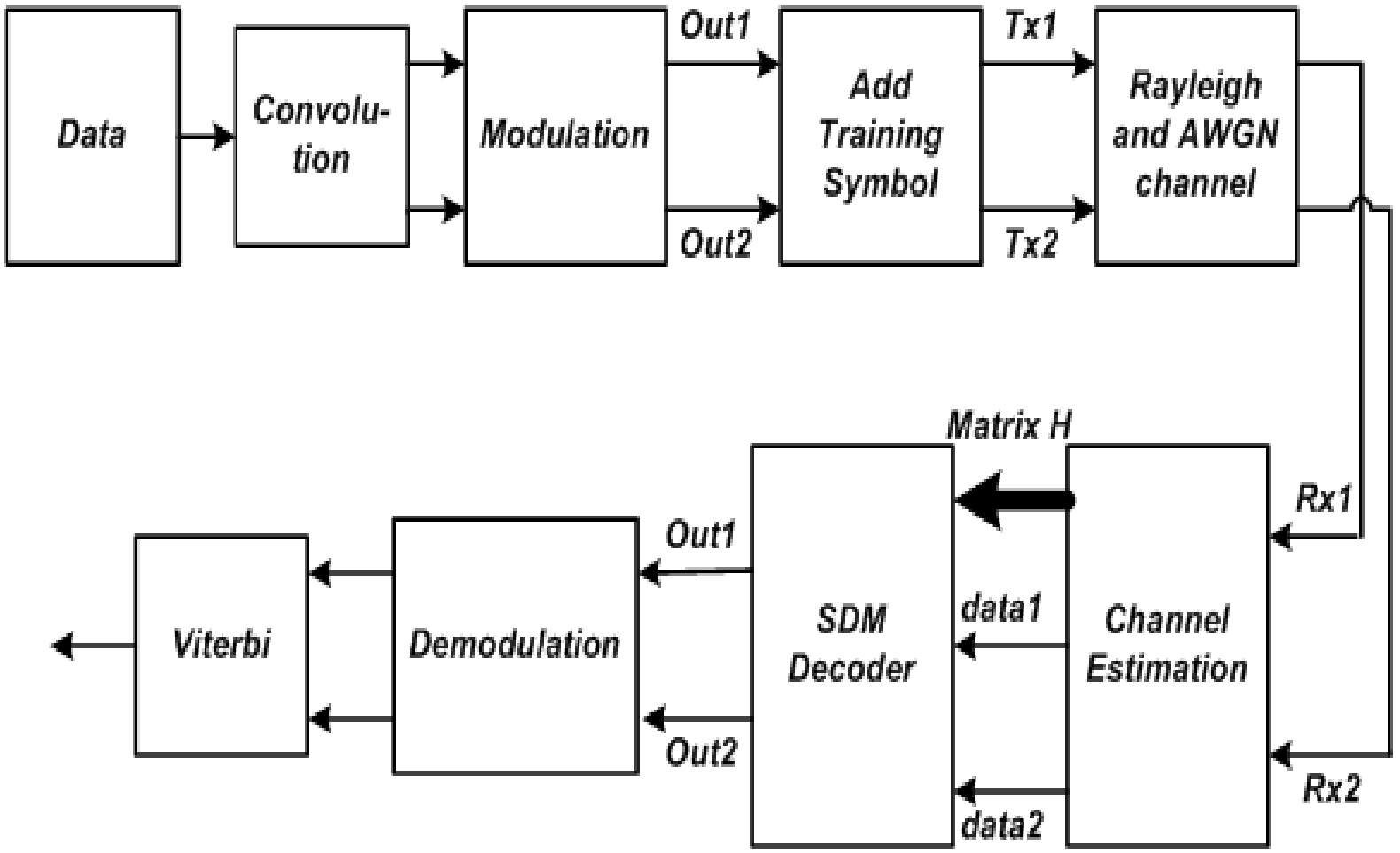
Design and Implementation of MIMO SDM Systems

Tools for designing:

Design Flow:

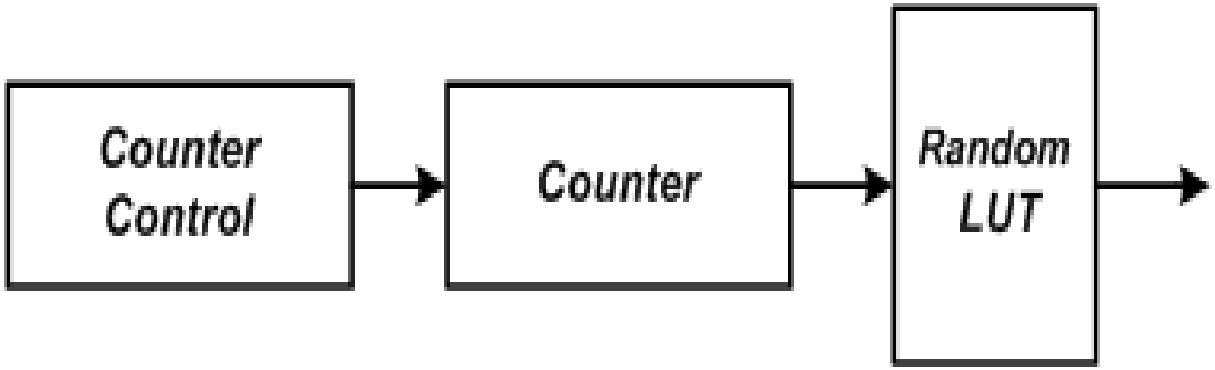


Design and Implementation of MIMO SDM Systems



Design and Implementation of MIMO SDM Systems

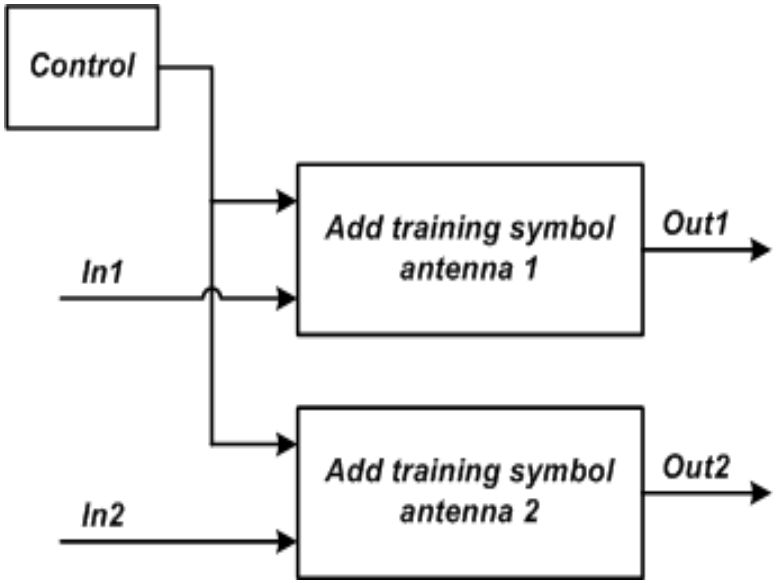
Data Generating:



Main activities:

- Bits Generator
- Control data rate

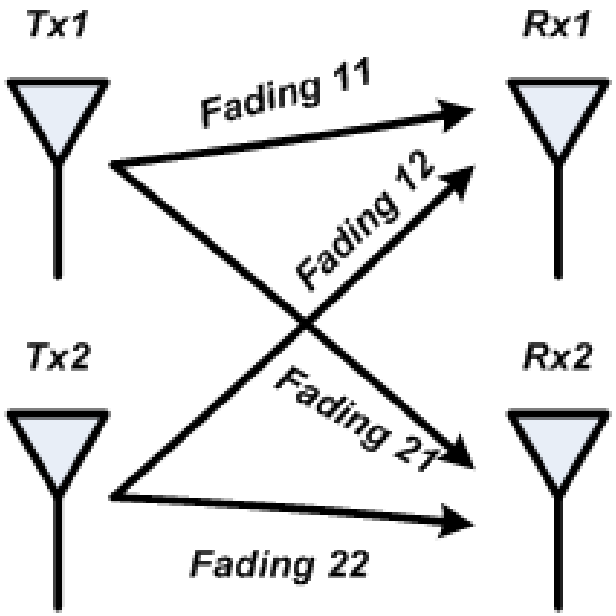
Design and Implementation of MIMO SDM Systems

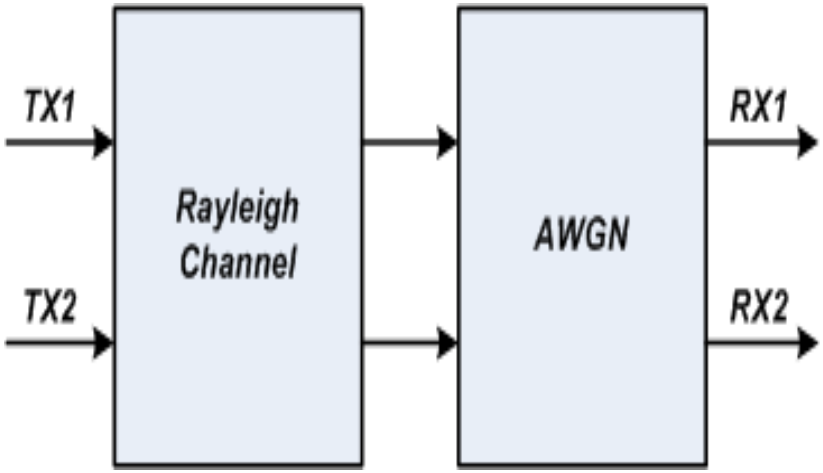


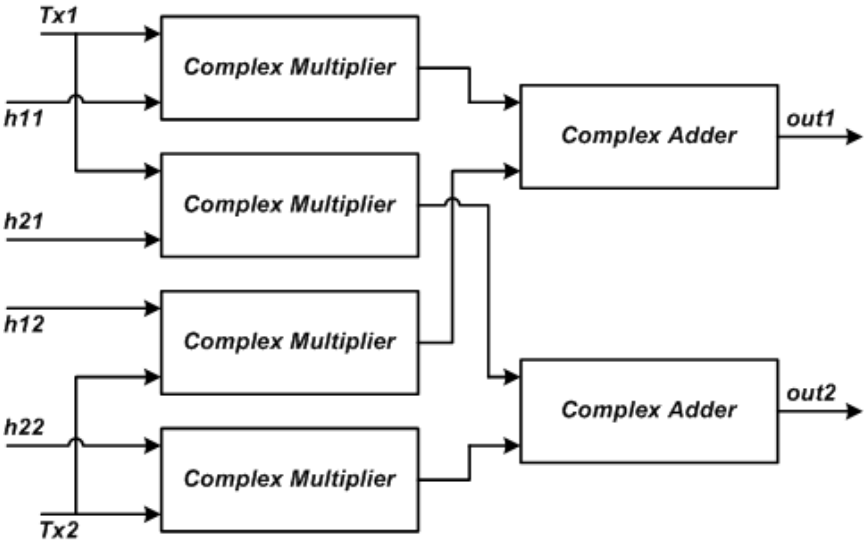
Data training symbol inserting module

Design and Implementation of MIMO SDM Systems

Channel:

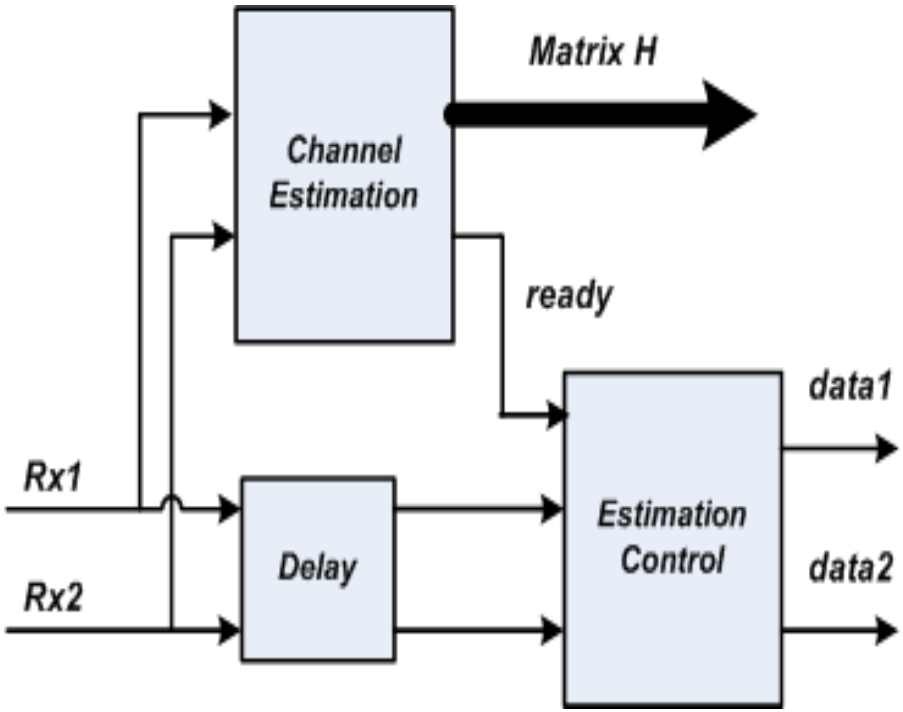


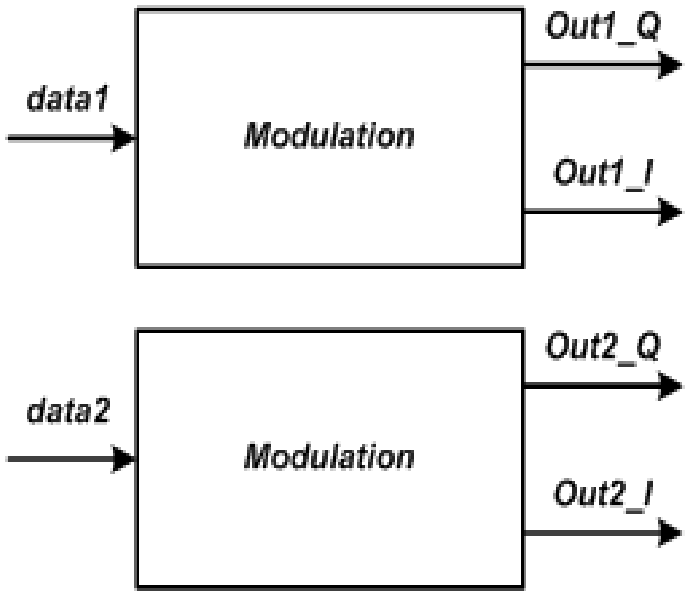




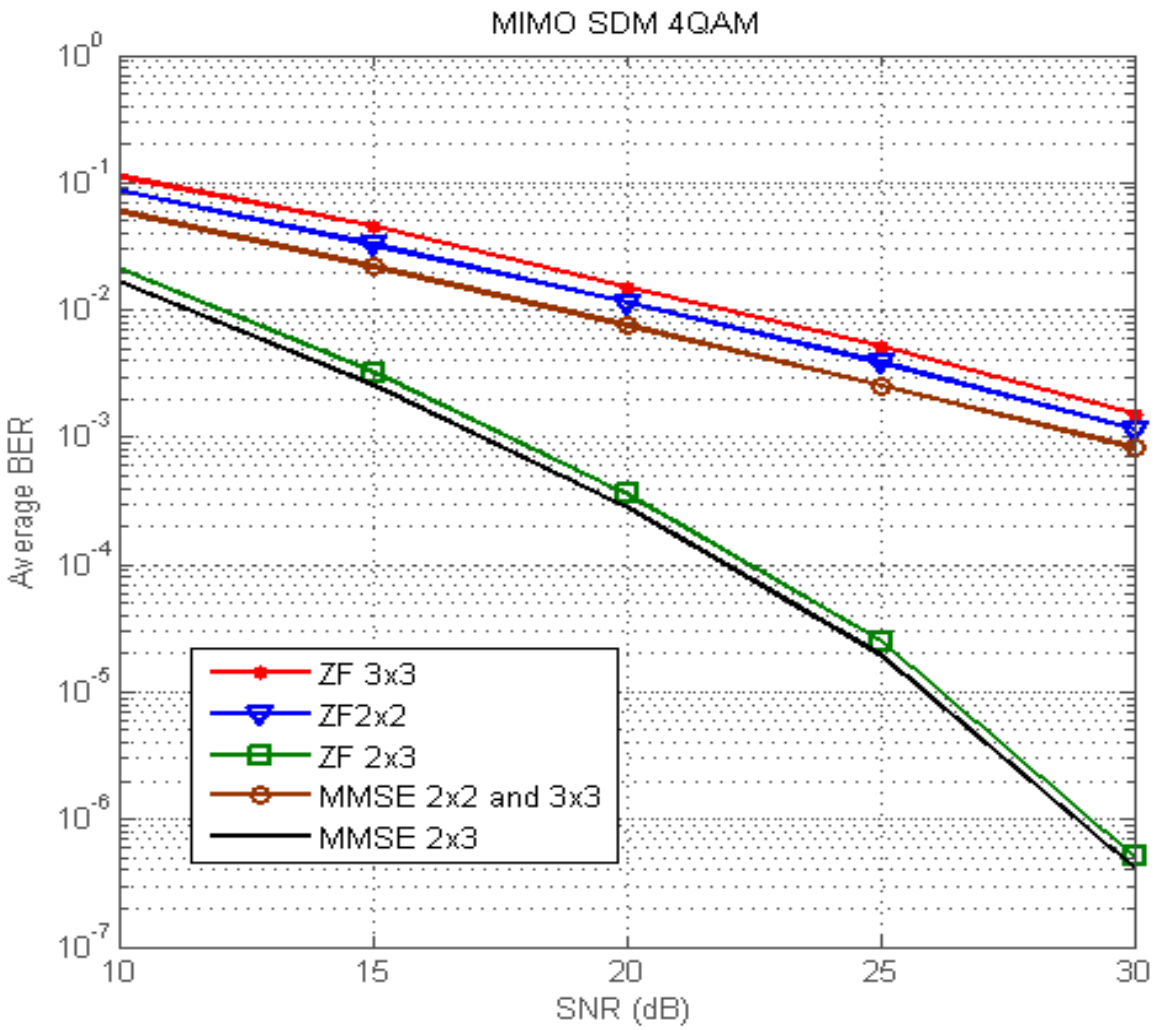
- Flat fading channel
- Additive white Gaussian noise

Design and Implementation of MIMO SDM Systems





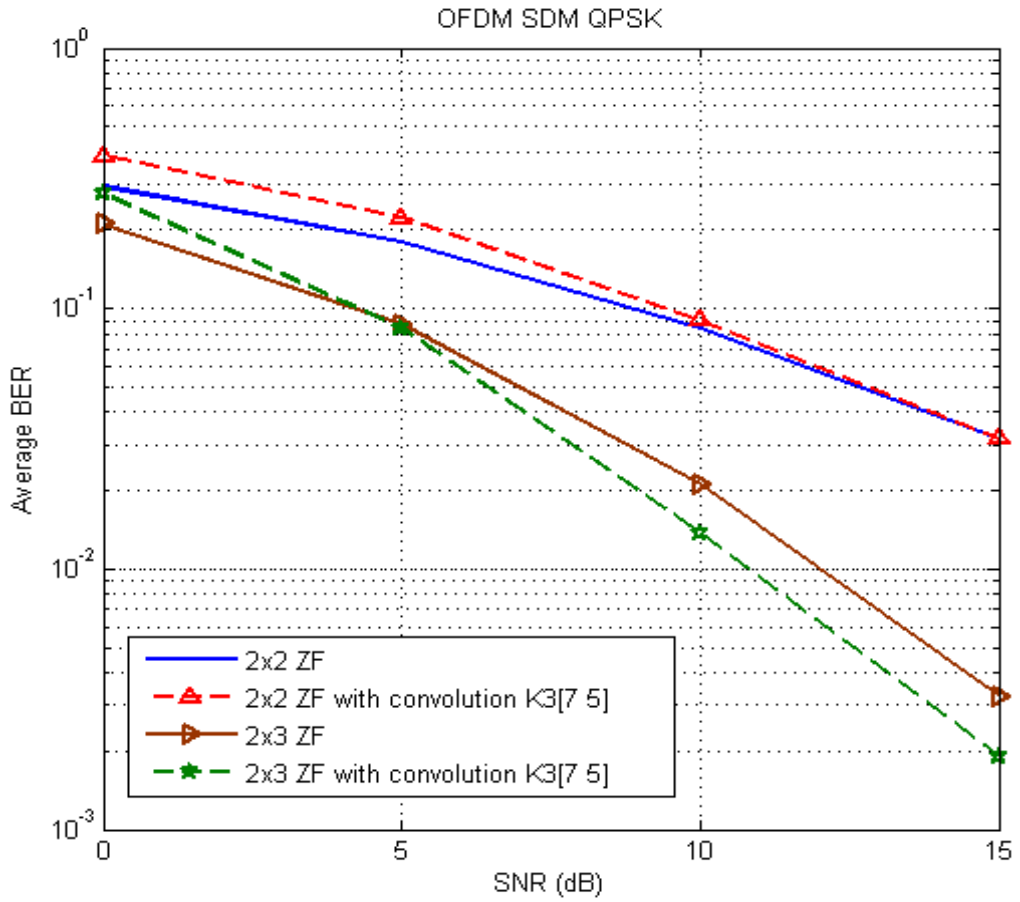
Results of Design and Implementation



BER performance of designed MIMO-SDM systems

(no channel coding)

Results of Design and Implementation



BER performance of designed MIMO-SDM systems (with channel coding)

Results of Design and Implementation

Hardware consumptions in the design of 2x2 MIMO SDM system used FPGA Stratix III 3SL150F1152C

Block	Consumption			
	The number in Model	Max Speed (MHz)	Combinational ALUTs Max:113,600	Dedicated Logic Registers Max:113,600
Modulation	2	420	0 (0%)	20 (<1%)
Demodulation	1	416.32	11 (<1%)	4 (<1%)
Add training symbol	2	420	18 (<1%)	2 (<1%)
SDM decoder	2	243.72	15 (<1%)	74 (<1%)
Channel estimation	1	162.60	22,519 (20%)	19,596 (17%)
Estimation control	1	147.12	3,530 (3%)	7,505 (7%)
Viterbi	1	206.06	20 (<1%)	141 (<1%)
Total evaluation		**147.12**	**<30%**	**<31%**

Conclusions

- In the paper, we have shown our design and implementation of MIMO SDM systems on FPGA hardware.
- Results have shown our successful in the design and implementation
- The maximum speed obtained is 147 MHz with hardware consumptions about 30%

Thanks you !

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